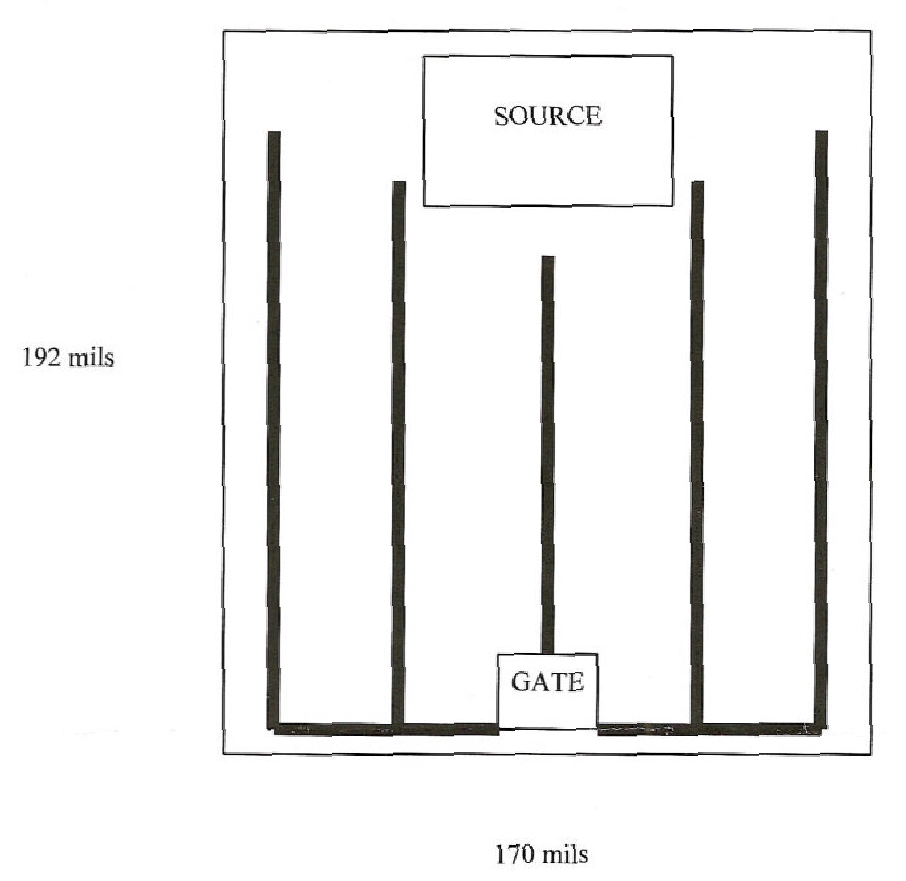
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**CHIP BACK IS DRAIN**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .042” X .060” G = .018” X .025”**

**Backside Potential: Drain**

**Mask Ref: Hex-4 100V GEN III**

**APPROVED BY: DK DIE SIZE .170” X .192” DATE: 7/11/22**

**MFG: IR THICKNESS .016” P/N: IRFC140**

**DG 10.1.2**

#### Rev B, 7/19/02